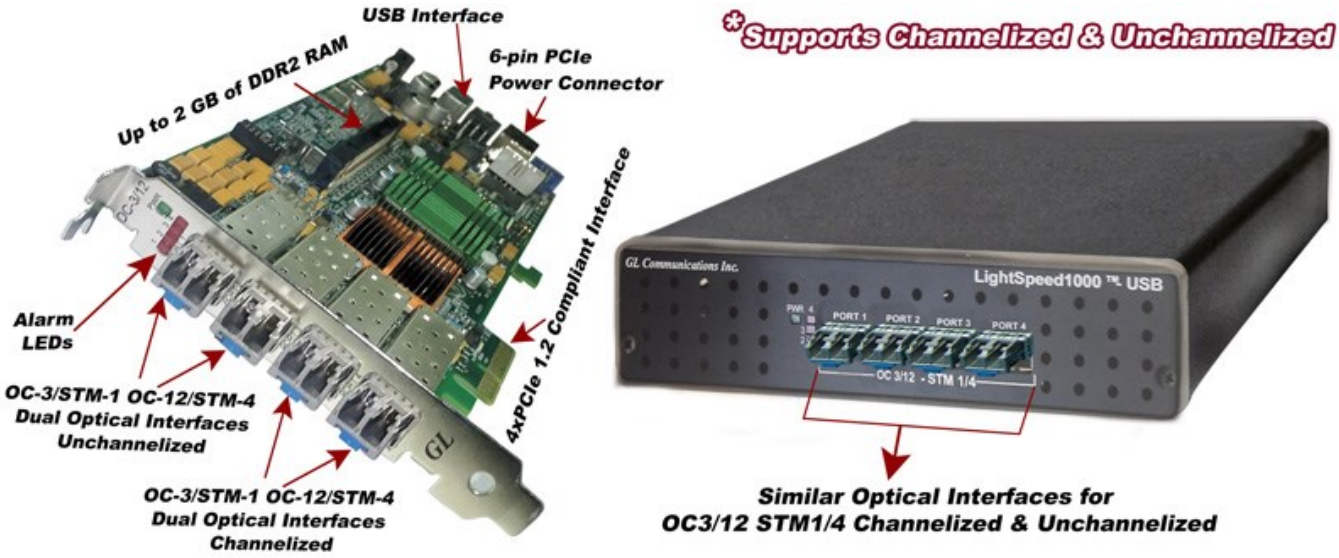
LightSpeed1000™(w/ GigE and USB 2.0)
(Legacy Product)

(OC-3/STM-1, OC-12/STM-4 Analysis and Emulation Card)



Overview

GL's LightSpeed1000™ hardware platform (available as PCIe Card and USB Pod) is capable of OC-3/12 and STM-1/4 wirespeed processing on quad optical ports for functions such as wirespeed recording and wirespeed playback of Unchannelized and Channelized ATM, PoS, RAW Traffic. Two ports out of the 4 ports are meant for SONET/SDH unchannelized and unframed data. The remaining two ports are meant for SONET/SDH channelized data of carrying many independent unframed/framed T1, E1, T3, and E3 streams

The LightSpeed1000™ comes with software for overall monitoring, BERT, emulation, and protocol analysis with a price tag that compares very favorably with similar test instruments at three times the price. In an OC-3/STM-1, all 84 T1s or all 63 E1s can be identified and processed in transmit and receive modes. In an OC-12/STM-4, all 336 T1s or all 252 E1s can be identified and processed in transmit and receive modes.

The hardware can also be easily configured / programmed for delaying of ATM Cells or PPP packets. The card's multiple connectivity using PCIe, Gigabit Ethernet (GigE), USB 2.0, and onboard DDR2 memory makes it suitable for various applications.

For more details, refer LightSpeed1000™ webpage.

Main Features

Hardware ED-137 Signaling Simulation

- *Multiple cards per system for super high capacity monitoring and test system
- High performance x4 PCIe interface with optimized DMA to perform Rx and Tx packets to/from PC memory
- Hardware based precise time-stamping of cells with 10 nsec resolution, 1 ppm accuracy

Analyzer Features

- Software selectable OC-3 / OC-12, or STM-1 / STM-4 for **Unchannelized** ATM, PoS or Transparent Traffic, and **Channelized** T1, E1, T3, E3 traffic
- API Toolkit to develop user specific applications

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Main Features (*Contd.*)

Traffic

- *Wirespeed processing of ATM, PoS or RAW data for Tx and Rx for both ports
- *Precisely emulates packet delays that occur over SONET/SDH carrying ATM or PoS traffic, delay is adjustable from 1 ms to maximum of 500 msec
- Ability to capture/playback to/from disk at full rate in both directions for all ports for detailed offline analysis
- Simultaneous synchronous capture or transmit is possible on all optical ports
- Comprehensive transmit/receive testing capabilities; transmitting and verifying data with incrementing sequence numbers with each packet/cell

BERT

- Easy to use and flexible Bit Error Rate Test (BERT) application for ATM, POS, and RAW

Protocol Testing

- ATM (AAL2, AAL5) Protocol Analyzer, UMTS Protocol Analyzer, PPP (IP and higher layer protocols) Protocol Analyzer

*PCIe card only

PoS Analyzer– Packet Over SONET / SDH

Overview

PoS, or Packet over SONET / SDH—OC-3/STM-1 and OC-12/STM-4 is supported at full rates over. Access, capture, analysis, and emulation of PPP and HDLC, all carrying IP traffic in real-time makes this card useful to many applications including routing, deep packet inspection, and other internet traffic applications.

PoS Protocol Analysis

PPP Analyzer can be used to capture a host of PPP protocols exchanged between the two nodes over SONET/SDH link. User can obtain detailed analysis of higher later protocols (IP, TCP, UDP, HTTP, FTP, POP3 etc.) and can perform various statistics measurements. Integrated Packet Data Analysis (PDA) in Real-time PPP Analyzer is an outstanding tool for live monitoring of VoIP traffic. It can segregate IP traffic into SIP / H323 / MEGACO / MGCP calls and collects statistics, CDRs, ladder diagrams, and a host of other useful information about VoIP calls.

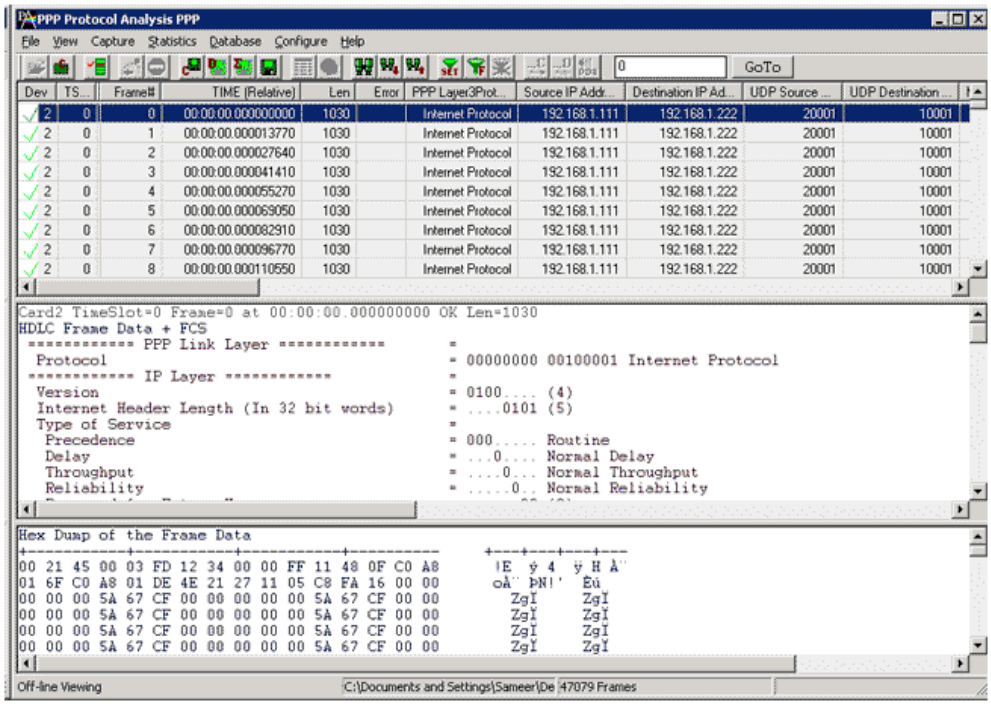


Figure: PPP Protocol Analyzer

PoS Port Configuration

PoS Port Configuration allows users to select FCS type, control FCS stripping on Rx and FCS appending on Tx.

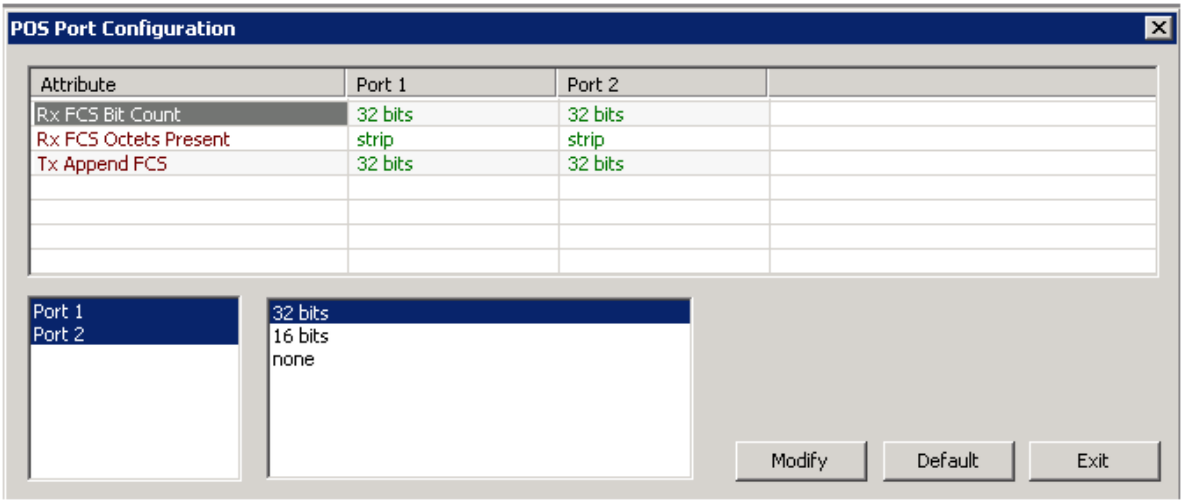


Figure: PoS Port Configuration

PoS BERT

Support for the following PRBS Patterns: 2^9 – 1, 2^11 – 1, 2^15 – 1, 2^20 – 1, 2^23 – 1, 2^29 – 1, 2^31 – 1, all one's, all zero's, alternate ones and zeros, user-defined pattern of lengths from 2 to 32 bits, invert and non-invert selections, single bit error insertion, error insert rate from 10^-1 to 10^-9, status for pattern sync, bit errors counters, and packet rate and packet gap configuration options, configurable header lengths and header information.

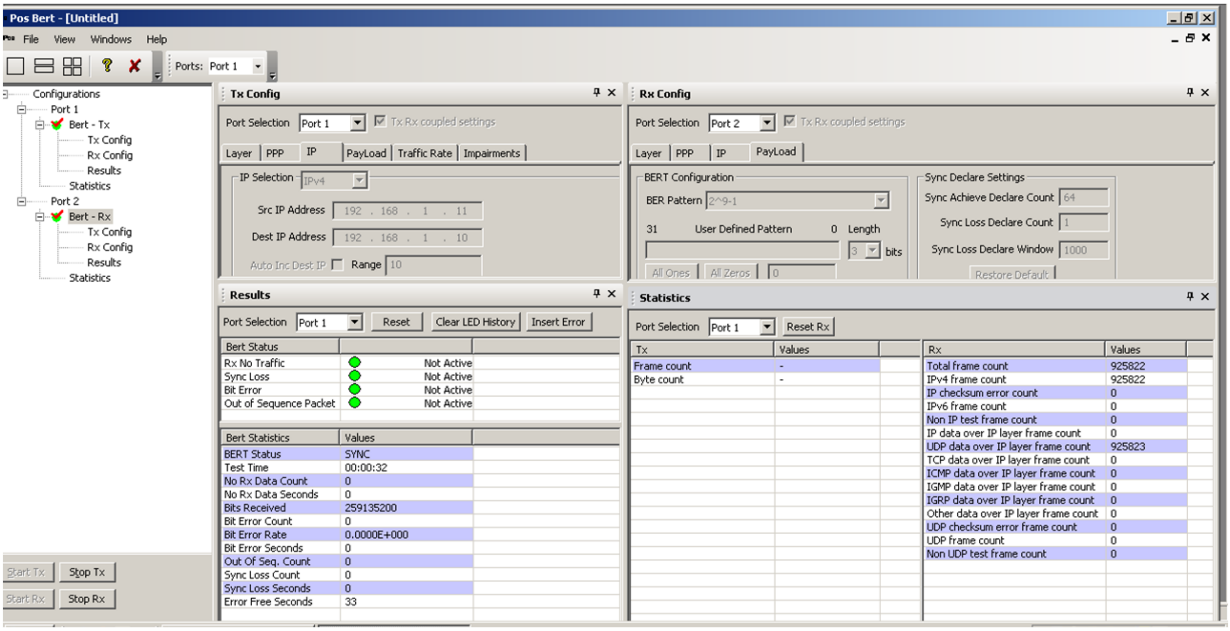


Figure: PoS BERT

PoS Tx / Rx Test

An emulation and test capability that transmits fixed, random, or variable lengths test packets and checks packets on receive at a user specified data transmission rate.

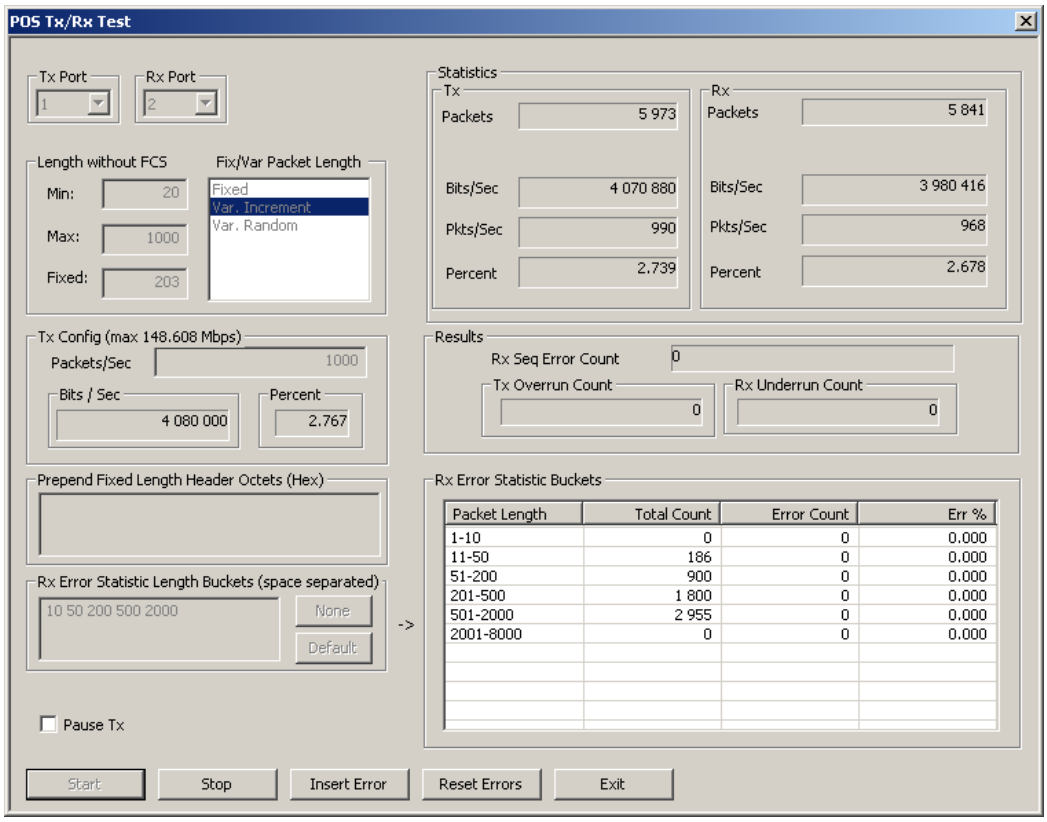


Figure: PoS Tx/Rx Test

ATM Analyzer– Asynchronous Transfer Mode Over SONET / SDH

Overview

ATM over SONT/SDH— OC-3/STM-1 and OC-12/STM-4 is supported at full rates. Access, capture, analysis, and emulation of ATM cells at wirespeed make this interface capability applicable for wide ranging next generation networks.

ATM Protocol Analyzer

ATM Analyzer is used to analyze and view ATM protocols across the U-plane for both NNI and UNI interface carrying AAL0, AAL2 and AAL5 traffic.

UMTS Protocol Analyzer

UMTS analyzer is capable of capturing, decoding and performing various test measurements across various interfaces i.e. Iub, Iur, IuCs and IuPs interfaces of the UMTS network. In addition, it supports ATM as the transport layer. It helps in fault diagnosis and troubleshooting UMTS network.

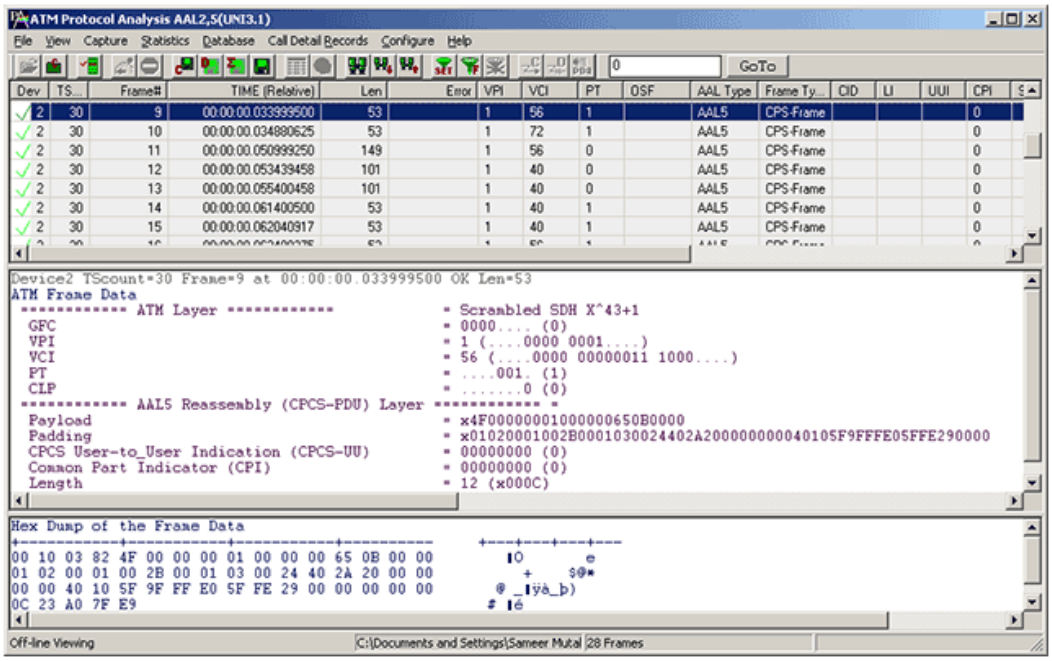


Figure: ATM Protocol Analyzer

ATM Configuration

ATM Configuration allows user to either pass or drop the Idle cells at the receiving stream.

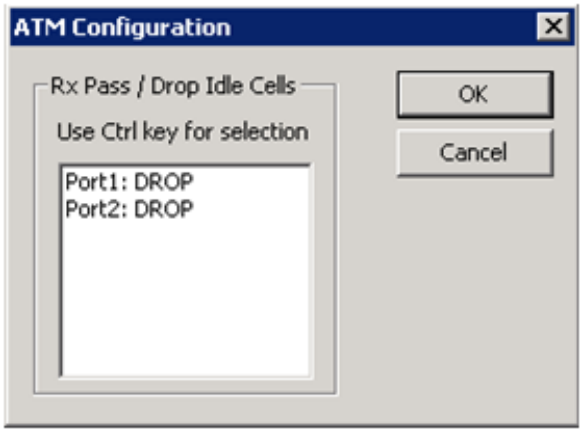


Figure: ATM Port Configuration

ATM BERT

Support for the following PRBS Patterns: 2^9 -1, 2^{11} -1, 2^{15} -1, 2^{20} -1, 2^{23} -1, 2^{29} -1, 2^{31} -1, All one's, all zero's, alternate ones and zeros, user defined pattern of lengths from 2 to 32 bits, invert and non-invert selections, single bit error insertion, error insert rate from 10^{-1} to 10^{-9}, HEC error insertion, on receive filtering is provided for idle cells, GFC, VPI, VCI, CL, and PT cells, statistical details for total cells, valid cells, idle cells, filtered cells, and filtered out cells.

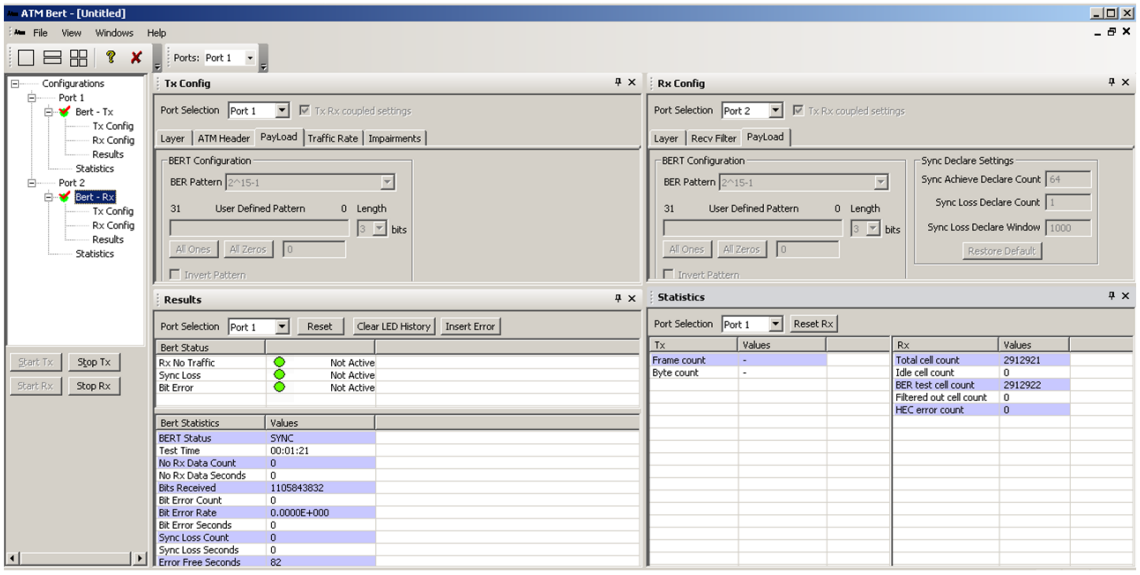


Figure: ATM BERT

ATM Tx / Rx Test

An emulation and test capability that transmits ATM test cells and / or analyzes the received cells at a user specified data transmission rate

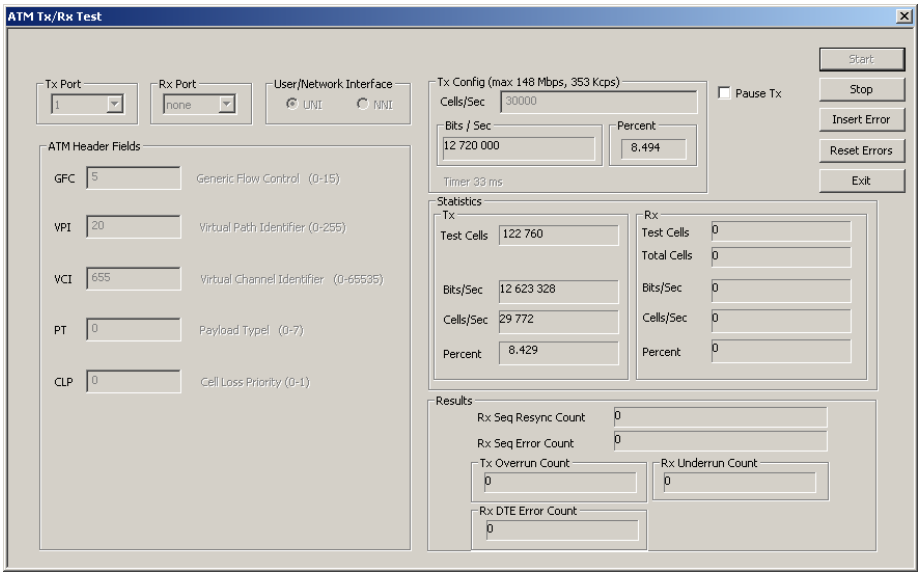


Figure: ATM Tx/Rx Test

Other Applications in LightSpeed1000™ Analyzer

Record, Playback Packets and Cells

These modules allow users to transmit and capture packets from file or to a file over OC-3/STM-1 and OC-12/STM-4 interfaces. Offline utility can convert it into GL's HDL file format or PCAP format.

Transmit Packets from File

- Transmits packets / cells from the file
- Packets can be transmitted either continuously, limited by number of packets/cells, or till the end of file (EOF)
- Transmit packets/cells at a user configurable rate
- Transmits on the same port as captured, swaps ports or uses a specified port
- Provides the statistics of the transmitted cells at both line level and payload level
- Transmit packets synchronously on multiple boards

Receive Packets to File

- Hardware provided **versatile multiple filters** can be applied to incoming data on each individual port to allow traffic of interest only. ATM and PoS traffic can be filtered at hardware level to target traffic of interest only
- Allows Wirespeed capture of all payload from SONET/SDH envelop transparent of transport level
- Captures the received packets synchronously on multiple boards into a file up to hard drive capacity
- Packets can be captured continuously (till user manually stops the capture or up to hard drive capacity) or limited by a specified size in MB, a packet count, or a specified time limit

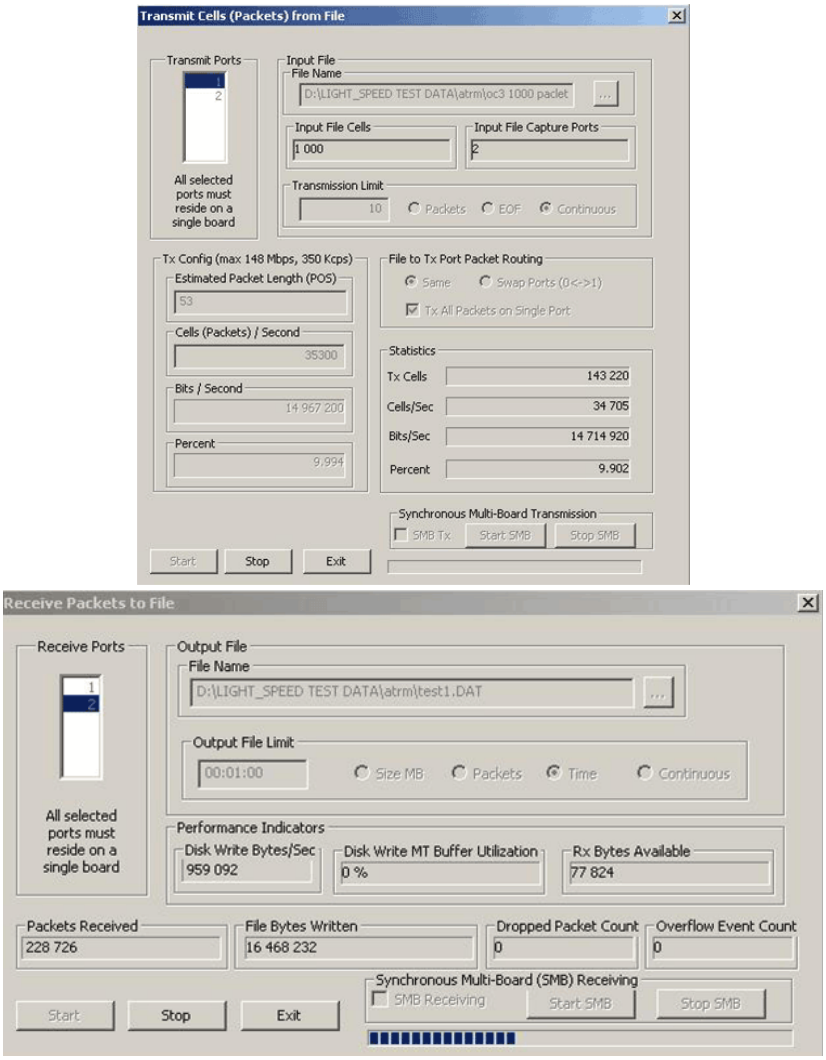


Figure: Receive Packets to File, Transmit Packets from File

Software Loopback (Rx-To-Tx Memory Loopback)

This application is used for diagnostic purposes. It loops all the received packets / cells from the SONET to the transmitting ports and displays the Tx and Rx information. Memory Loopback application uses both ports on the selected board.

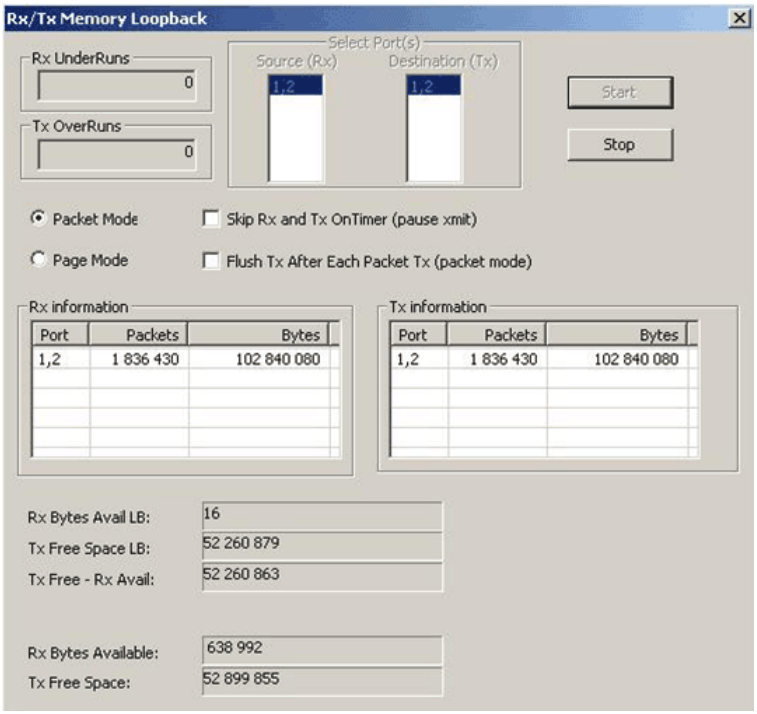


Figure: Memory Loopback

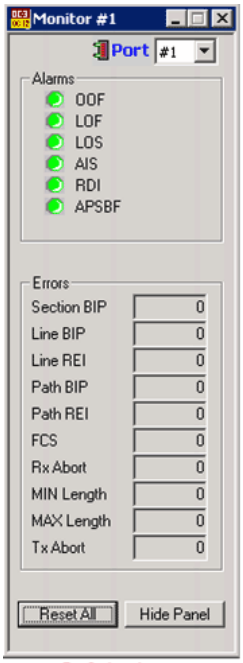
Alarms and Errors Counters Monitoring

The alarms and error monitoring window provided for each of the OC-3/OC-12 port displays detailed status of the communication with the other end.

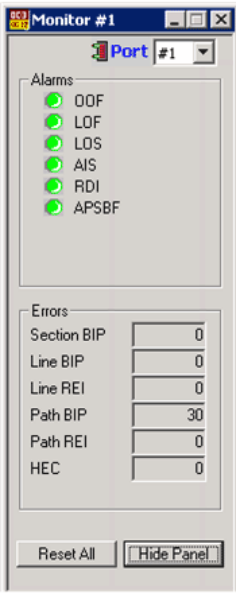
Hardware LEDs are provided on the card to read line alarms.

Monitored Alarms and error counts include –

- Line errors such as OOF, LOS, LOF, AIS, RDI, and APSBF
- FCS, Rx / Tx Abort, and MIN / MAX Length
- Line, Path, and Section error counts



PoS Analyzer Monitor Panel



ATM Analyzer Monitor Panel

SONET/SDH RAW (or Transparent) Payload

RAW mode captures or playbacks anything and everything on SONET/SDH. This mode allows capturing/replaying including SONET/SDH Framing and payload. Here payload can be anything, including structured traffic (T1, E1, STS-1, DS3 etc) or unstructured traffic (ATM, PoS, GFP etc). Raw or transparent mode allows direct access to the SONET / SDH payload for BERT, data transmit and receive applications. Current applications include:

- **RAW BERT** – support for the following PRBS Patterns: $2^9 - 1$, $2^{11} - 1$, $2^{15} - 1$, $2^{20} - 1$, $2^{23} - 1$, $2^{29} - 1$, $2^{31} - 1$, all one's, all zero's, alternate ones and zeros, user defined pattern of lengths from 2 to 32 bits, invert and non-invert selections, single bit error insertion, error insert rate from 10^{-1} to 10^{-9}, status for pattern sync, and bit errors counters
- **Wirespeed capture of raw data** to hard disk on one or both ports simultaneously. The data is recorded in 64 bytes block with appropriate header
- **Playback of recorded data** from file at wirespeed on one or both ports
- **Alarms and Error** monitoring and logging at SONET/SDH level

Performance Counters

Following performance counters are available in the analyzer: Tx Statistics, Rx Statistics, PMC TxRx Statistics, Interrupt Statistics, and DMA Engine. The statistics display two types of counters: board counters and port counters. The board counters display cumulative counts for all ports on the same board, while port counters display information for each port separately.

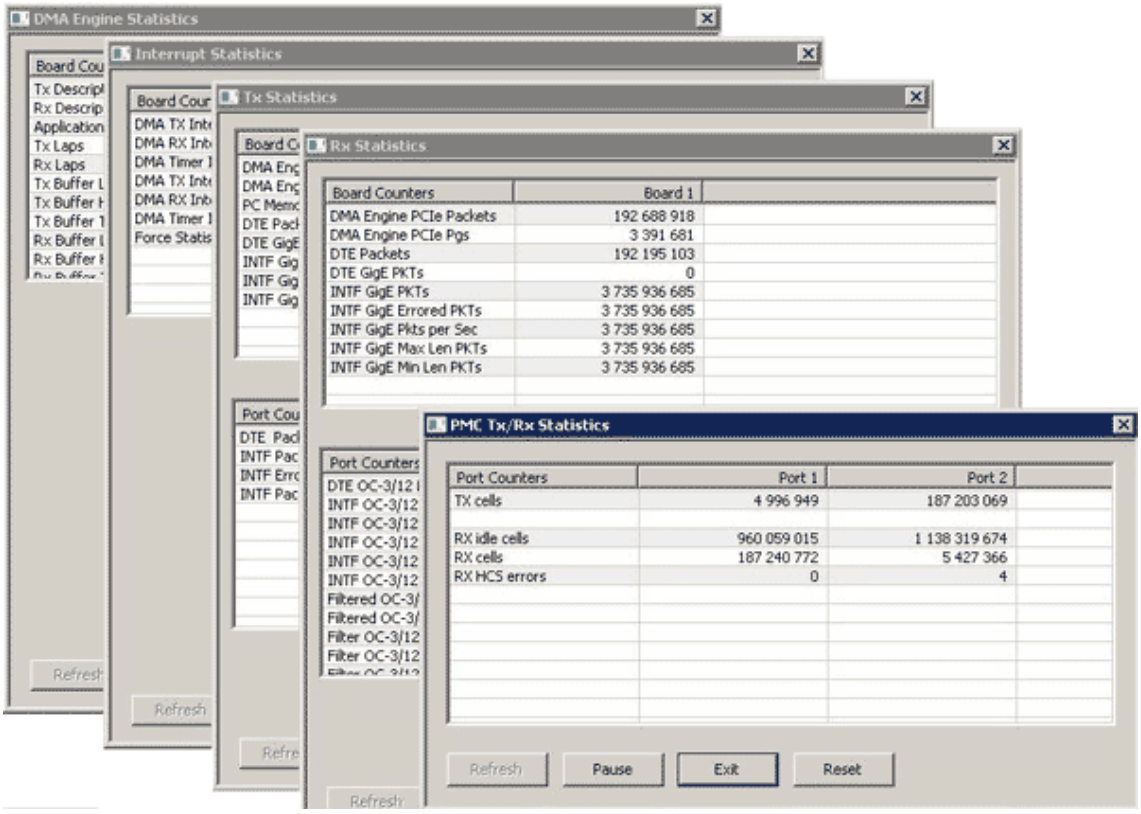


Figure: Packet Delay Emulation

Software Loopback (Rx-To-Tx Memory Loopback)

This application is used for diagnostic purposes. It loops all the received packets / cells from the SONET to the transmitting ports and displays the Tx and Rx information. Memory Loopback application uses both ports on the selected board.

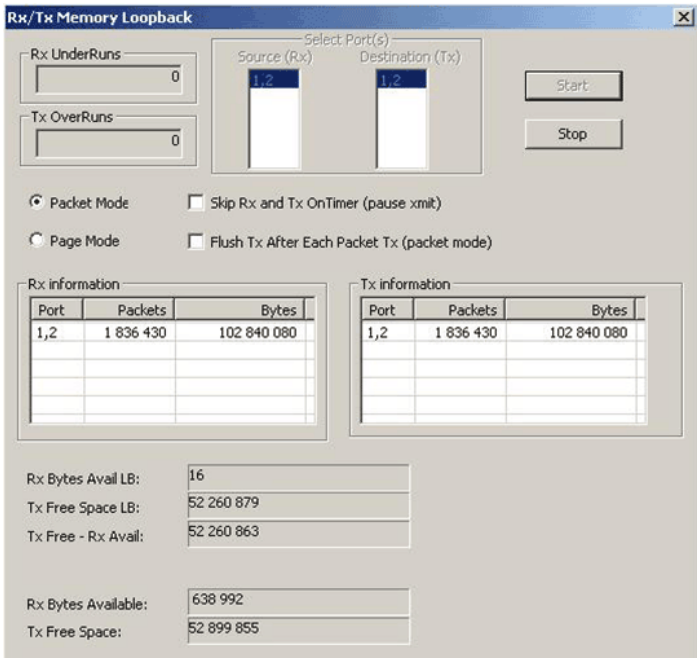


Figure: Memory Loopback

Packet Delay Emulation for PoS and ATM based traffic

The Network Delay Emulator is an optional application (requires license) provides full duplex delay simulation for PoS and ATM based traffic from 1 ms to 500 ms, with incremental delays of 1 ms. The application combines hardware and software based functions to achieve precision and flexibility. It can emulate packet delays that occur over SONET/SDH carrying ATM/PoS traffic.

With this application, the user can:

- Test the impact of delay and congestion under various real world conditions
- Assess impact of delay on SLA (Service Level Agreements),
- Simulate satellite delay and long Fiber Loops
- Test WAN application performance under deteriorated but repeatable conditions

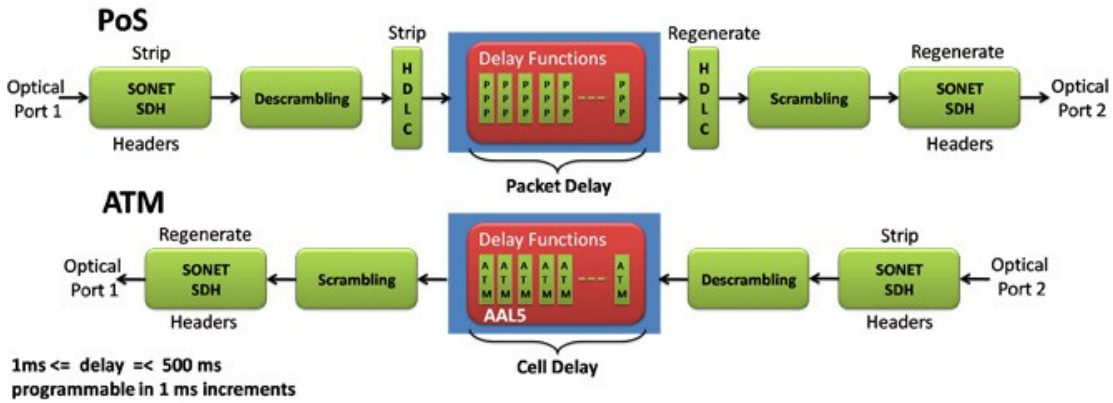


Figure: Packet Delay Emulation

Supported Protocols

- **ATM –** Implements the ATM Forum User Network Interface Specification and the ATM physical layer for Broadband ISDN according to CCITT Recommendation I.432
- **PPP over SONET (PoS)** – Implements the Point-to-Point Protocol (PPP) over SONET / SDH specification according to RFC 2615 (1619) / 1662 of the PPP Working Group of the Internet Engineering Task Force (IETF)
- **OC-3/OC-12/STM-1/STM-4 Transparent Payload** – Analyzer processes SONET/SDH payload in transparent (RAW) mode without any transport protocols

Specifications

Interfaces:

- 2 x Unchannelized OC-3 / STM-1 / OC-12 / STM-4 Ports (Port 1 Port 2)
- 2 x Channelized OC-3 / STM-1 / OC-12 / STM-4 Ports (Port 3 Port 4)
- Single Mode or Multi Mode SFP support with LC connector

Protocols:

- POS compliance specs - RFC 2615(1619)/1662

Tx Clock

- Internal or Recovered

Alarm LEDs:

- LOS, LOF, User

Bus Interface:

- PCIe Specification
  - 1.2 Compliant
- USB 2.0

Power and Dimensions:

- +12 volts, 3.5 Amps
- 4.2” x 9.2”

Buyer's Guide

Item No	Product Description
LTS100	Lightspeed1000™ - Dual OC-3/12 STM-1/4 PCIe Card
LTS105	Lightspeed1000™ - Portable Dual OC-3/12 STM-1/4 USB Unit
IPN1310a	SFP Transceiver for OC-3/STM-1 and OC-12/STM-4 Optical, LC, Single-Mode, 1310nm
IPN850a	SFP Transceiver for OC-3/STM-1 and OC-12/STM-4 Optical, LC, Multi-Mode, 850 nm or 1310 nm

Item No	Unchannelized Analysis and Emulation Applications Related Software
LTS200	OC-3/STM-1 ATM Monitor, BERT, Tx/Rx Test, RAW
LTS300	OC-12/STM-4 ATM Monitor, BERT, Tx/Rx Test, RAW
LTS201	OC-3/STM-1 PoS Monitor, BERT, Tx/Rx Test, RAW
LTS301	OC-12/STM-4 PoS Monitor, BERT, Tx/Rx Test, RAW
LTS202	OC-3/STM-1 ATM and RAW Record / Playback
LTS203	OC-3/STM-1 PoS and RAW Record / Playback
LTS302	OC-12/STM-4 ATM and RAW Record / Playback
LTS303	OC-12/STM-4 PoS and RAW Record / Playback
LTS204	OC-3/STM-1 ATM Protocol Analysis
LTS304	OC-12/STM-4 ATM Protocol Analysis
LTS206	OC-3/STM-1 UMTS Protocol Analysis
LTS306	OC-12/STM-4 UMTS Protocol Analysis
LTS215	Packet Data Analysis (PDA) for PoS
LTS207	Delay Emulation for OC-3/STM-1 PoS payloads
LTS208	Delay Emulation for OC-3/STM-1 ATM payloads
LTS307	Delay Emulation for OC-12/STM-4 PoS payloads
LTS308	Delay Emulation for OC-12/STM-4 ATM payloads

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Buyer's Guide (*Contd.*)

Item No	OC-12 / STM-4 Related Software Related Hardware
LTS501	OC-3/STM-1 RAW
LTS502	OC-12/STM-4 RAW
LTS503	Record Playback for OC-3/STM-1 RAW
LTS504	Record Playback for OC-4/STM-4 RAW
LTS108	Any 16 Ports Channelized License for OC-3/STM-1
LTS116	Any 32 Ports Channelized License for OC-3/STM-1
LTS124	Any 48 Ports Channelized License for OC-3/STM-1
LTS132	Any 64 Ports Channelized License for OC-3/STM-1
LTS164	All Ports Channelized Licenses for OC-3/STM-1 (84x2 for T1, 63x2 for E1)

Note: PCs which include GL hardware/software require Intel or AMD processors for compliance.

For more details, refer LightSpeed1000™ webpage.

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